cept for the input of filter **62** since its output is directed only to the input of the AND gate **71**, and with the exception of the EXCLUSIVE NOR gates **69** whose function is also a function of another attribute **65**, all of which must occur simultaneously along with a true bit output from the filter **68** as well as other system logics **66'**. Although the illustrative circuit in FIG. **4** serves to show how the various possibilities in applying the concept and building blocks of the byte filter can be used in a specific way, it more importantly illustrates the endless variance possible in accordance with the concepts and approach utilized in this invention.

In regard to FIG. **4** which illustrates different variations in logical output, no attempt has been made to illustrate conservation in elements or other potential connections which would yield the same logical output. For example, if the column of filters **70** were removed from the position as shown in FIG. **4** and instead used to compare the n register stages **74** and the z register stages **78** at the respective inputs of the filter **70**, the outputs of which are then used as references to the filters **59, 62** and **63** instead of a direct connection to the n register stages **74** as shown, the output **72** would be equal to the same Boolean expression as the output illustrated in FIG. **4**. Again, the concept of the filter with a memory reference which memory can be a temporary register that can be clocked to change the value of the reference is a feature of the present invention and not the various connections which are only illustrative examples to demonstrate the invention, its usefulness and operation.

FIG. **5** illustrates an interconnection of a plurality of building blocks which were used in FIG. **4** to decode a group of n inputs with an output corresponding to a successful decoding of that group to create a hypothetical hierarchal structure, which of course, may be varied at the desire of the designer. In order to simplify the illustration of FIG. **5**, all filter groups are assumed to have the same characteristics as those illustrated in FIG. **4**. Filters **83, 85** and **87**, having filter Group I, II and III inputs **82, 84** and **86** respectively, the outputs **92, 93** and **94** of which feed into a filter **96** where along with other inputs **95** are compared with the memory register x. To pass the filter **96** with true output **97**, the input Groups I, II, III must pass the second level of security represented by the code in register x of filter **96**. Similarly, to achieve a final output **102**, the original input Groups I, II and III must additionally pass the third level comparison of register y in filters **101**. These along with the second level test for inputs **88** and **90** from Groups IV and V, respectively, and inputs **95** to filter **96** and also inputs **100** to filter **101**.

In order to aid in understanding the rationale of the present invention, reference is now made to FIG. **6** which is a simplified version of FIG. **4** in which the registers are clocked as a direct result of input data. In FIG. **6** data bits 0, 1 and 2 are applied via data lines **61** to the input of EXCLUSIVE NOR gates **59, 62** and **63**, respectively, and at the same time to a logical NOR gate **60** which applies its output in the form of clock pulses N to a three stage ring register **74**. The register **74** produces reference outputs N_0, N_1 and N_2 which are applied to the reference input of EXCLUSIVE NOR gates **59, 62** and **63**, respectively. The clock pulse N is a combination of (data bit 0+ data bit 1+ data bit 2). Data bits 3, 4 and 5 are applied to AND gate **77** which generates a clock pulse Z equal to data bit 3×data bit 4× data bit **5** which is applied to the two stage ring register **78** having outputs Z_0 and Z_1 which are applied to the reference inputs of EXCLUSIVE NOR gates **70** as shown. One example of the loading of the registers as well as the data input bit vs output results with the registers loaded are shown in the Truth Table as follows:

TRUTH TABLE

Program Step No.	1st Six Data Bits 0 1 2 3 4 5	N Register Contents N_0 N_1 N_2	Z Register Contents Z_0 Z_1	Out
0	INITIAL LOADING	0 1 1	1 0	NA
1	1 0 1 1 0 1	0 1 1	1 0	0
2	1 1 1 0 0 0	0 1 1	1 0	0
3	0 0 0 1 0 1	1 0 1	1 0	0
4	0 1 0 1 1 1	1 0 1	0 1	0
5	0 0 0 1 1 0	1 1 0	0 1	0
6	0 1 0 1 1 0	1 1 0	0 1	1
7	0 1 0 1 1 1	1 1 0	1 0	0
8	0 1 0 1 1 0	1 1 0	1 0	0
9	1 1 1 0 1 0	1 1 0	1 0	1
10	0 0 0 1 1 1	0 1 1	0 1	0
Rerun same data				
1a	1 0 1 1 0 1	0 1 1	0 1	0
2a	1 1 1 0 0 0	0 1 1	0 1	1
3a	0 0 0 1 0 1	1 0 1	0 1	0
4a	0 1 0 1 1 1	1 0 1	1 0	0
5a	0 0 0 1 1 0	1 1 0	1 0	0
6a	0 1 0 1 1 0	1 1 0	1 0	0
7a	0 1 0 1 1 1	1 1 0	0 1	1
8a	0 1 0 1 1 0	1 1 0	0 1	1
9a	1 1 1 0 1 0	1 1 0	0 1	0
10a	0 0 0 1 1 1	0 1 1	1 0	0

The multi stage filter as illustrated in FIG. **6** may be plugged in or otherwise connected to the printer port of a computer, for example, a serial/parallel adapter **23** made by IBM. A typical address for such a printer port in an IBM compatible micro-computer operating in an MSDOS environment might by "888". In the specified adapter there are eight data bit lines so eight bits to a byte of which the last two are higher order bits (6 and 7) are arbitrary and have no purpose in the examples chosen for purposes of illustration. Accordingly, a typical program in BASIC takes the form of instruction; out "address", "byte value" provides signals appearing on the computer printer port as follows:

Program Step No.	Statement	Bit Values 1 Data Bits 0	2 1	4 2	8 3	16 4	32 5	64 6	128 7
1 Out	888,45 Yields	1	0	1	1	0	1	0	0
2 Out	888,71 Yields	1	1	1	0	0	0	1	0
3 Out	888,168 Yields	0	0	0	1	0	1	0	1
4 Out	888,250 Yields	0	1	0	1	1	1	1	1
5 Out	888,24 Yields	0	0	0	1	1	0	0	0
6 Out	888,90 Yields	0	1	0	1	1	0	1	0
7 Out	888,250 Yields	0	1	0	1	1	1	1	1
8 Out	888,154 Yields	0	1	0	1	1	0	0	1
9 Out	888,87 Yields	1	1	1	0	1	0	1	0
10 Out	888,56 Yields	0	0	0	1	1	1	0	0

As will be noted these correspond to the examples chosen in the Truth Tables for the operation and application to the filter network of FIG. **6**. The outputs generated from that filter network may be connected to an acknowledgement line, for examination by the computer or may be counted, accumulated and used in different manner until an additional result is achieved and